



Ultra High-Speed Acquisition Board



General

The UHAB (Ultra High-speed Acquisition Board) has both analog to digital and digital to analog converters on board as well as two Virtex-4 SX35 FPGAs, one for DSP and the other for data communication.

Features

- Dual 8bit 1.5 GSPS ADC
- Two 14bit 1.2 GSPS DACs
- Two Virtex-4 SX35 FPGAs
- Single 5V DC supply delivering around 3A (application specific)
- 100x160 Eurocard form factor (excl. backplane connector)
- Flexible communication solutions (optical & electrical Ethernet, RS232)
- Numerous number of digital I/O (>50 signals)
 - Ø Industrial temperature range (-40 to 100 °C)
 - Ø Supervision of temperature and power for all key components
 - Ø 32x4 Mbit 167MHz SDRAM & 4Mbit Serial FLASH (SPI) on board
 - Ø Optional memories: DDR2, and SD Card

APPLICATIONS

- Broadband communication systems
- Instrumentation, automatic test equipment
- Electronic Warfare (e.g. Radar)
- Direct RF Down Conversion
- Digital Oscilloscopes
- Satellite Set-top boxes
- Communication Systems
- Test Instrumentation

Analog In

One ADC08D1500 dual channel 8bit 1.5 GSPS ADC. Possible to use an interleave mode to get a single channel 3 GSPS converter.

Specifications :

ENOB = 7 to 7.4 SNR = 44.5 to 47 dB
THD = -54.5 to -47 dB SFDR = 56 to 48.5 dB

The two inputs are single ended AC coupled through SMA connectors. Two programmable attenuators -31 to 0 dB in 1dB steps.



Analog Out

Two 14bit AD9736 DACs capable of 1200 MSPS conversion rate.

Specifications :

- SFDR = 82 dBc at f_{OUT} = 30 MHz
- SFDR = 69 dBc at f_{OUT} = 130 MHz
- IMD = 87 dBc at f_{OUT} = 30 MHz
- IMD = 82 dBc at f_{OUT} = 130 MHz

Single ended SMA connector out, optional differential MMCX connectors.

DSP FPGA

There is one Xilinx Virtex-4 SX FPGA dedicated for DSP. Featuring 192 MACS in HW possible to run at 500MHz, 34,560 Logic Cells, 3.456 Mbit memory. It provides an interface to the ADC and the DAC.

COM FPGA

There is one FPGA, of the same type as the DSP FPGA, dedicated to data communication. It can also be used to extend the DSP capabilities of the DSP FPGA. The COM FPGA connects the OPTO module and the Mini-Module as well as all the memories, i.e. the SDRAM, serial FLASH and the SD Card socket. The two FPGAs are inter-connected through 20 high-speed LVDS pairs.

Digital I/O

SERCOM - Synchronous serial communication using LVDS via RJ-45 at 500Mbit/s total data rate. An extra single ended signal is provided for e.g. flow control.

DIG_SMA - The DSP FPGA has an MMCX connector that can be used as digital input/output, e.g. can be used as trigger.

DIG_MMCX - Each FPGA has a MMCX connector that can be used as digital input/output.

INTERCOM - A fine pitch (1.27) 26pin header provides 12

LVDS 250MBit/s pairs (3Gbit/s total capacity) for inter-connection to a second UHAB board, for e.g. synchronous handling of several channels.

TEST - Each FPGA has a 14pin header used for test purposes, e.g. carrying 6 differential pairs or 12 single ended signals.

Data Communication

RS232 - Two on each FPGA.

OPTO - 1Gbit/s Ethernet Opto link for data transfer of acquisition data to e.g. a PC over UDP protocol. The UDP protocol is implemented in HW in the COM FPGA, available as IP from BitSim.

Mini-Module

The board can be equipped with an optional Xilinx Virtex-4 FX12 Mini-Module. The module is based on a Virtex-4 FX12 FPGA with a built-in PowerPC. The module has a 10/100/1000 Ethernet Port via RJ-45, 32M x 16 DDR and 2M x 16 Flash. The 76 User I/O:s are connected to the COM FPGA and can be configured either as single ended or as LVDS differential pairs. The Mini-Module makes it easier to implement Internet connectivity on the UHAB.

FPGA Loading

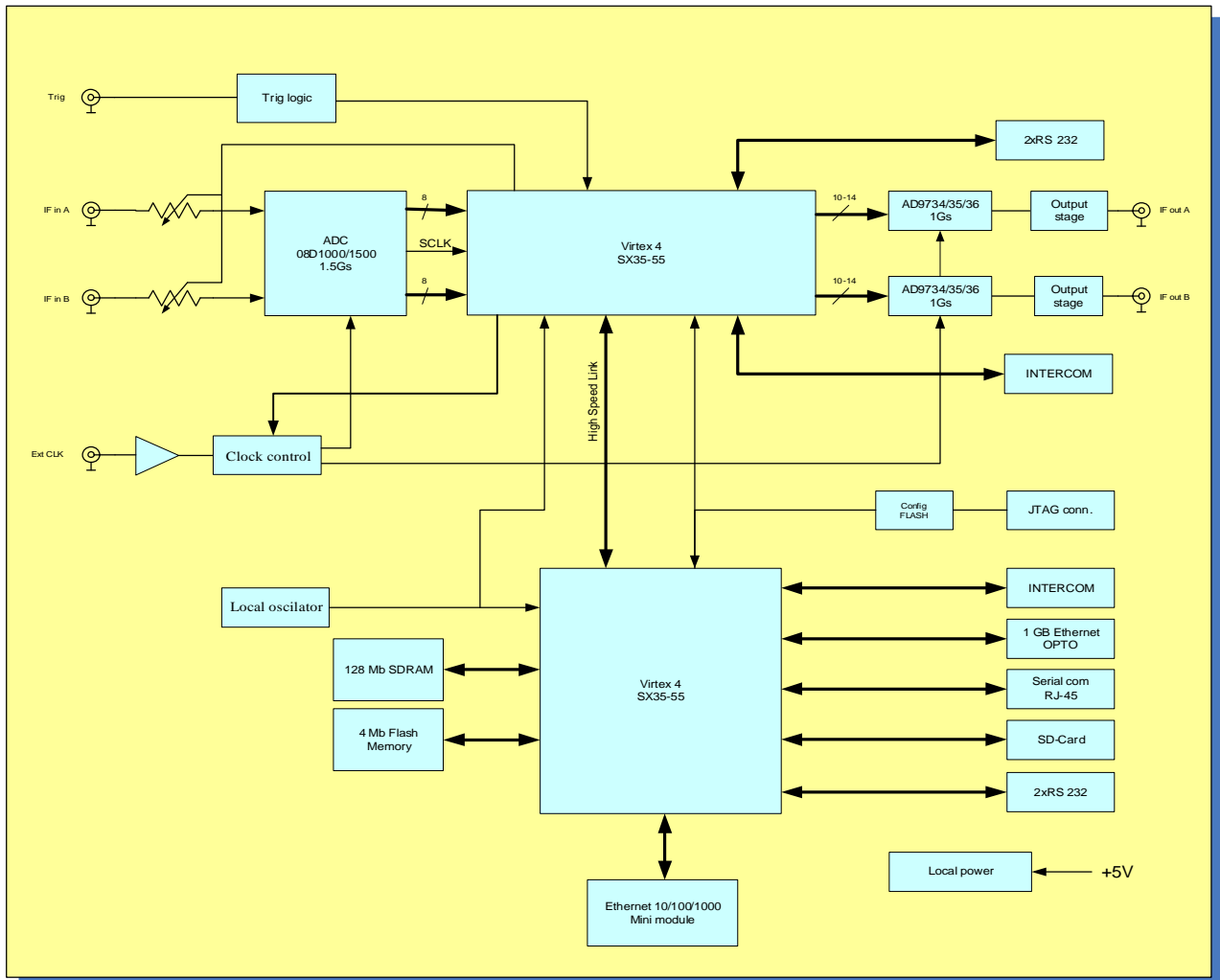
The FPGAs can be loaded in one of several ways. They can be loaded from the on-board configuration PROM at power-on, via the JTAG chain, or from the Mini-Module to facilitate remote update of the FPGAs via e.g. Ethernet LAN or Internet.

BSP (Bord Support Package)

BitSim provides a BSP that implements all of the framework needed to build a complete data acquisition system. The BSP consists of IPs for the interface blocks to the ADC & DACs. Optional IPs available such as UDP (in HW), RS232, and SERCOM etc. Other IPs can be added on request.

For more information on the UHAB-solution, contact: sales@bitsim.com

Block Diagram



Contact information

September 2006

Head Office
S:t Eriksgatan 63
SE 112 34 Stockholm
Sweden

Tel. +46 (0)8-54 55 56 00
Fax. +46(0)8-54 55 56 11
www.bitsim.com
sales@bitsim.com

Copyright © 2006 BitSim AB